IN THE SPECIFICATION

Please amend the specification as follows:

The paragraph beginning at page 20, line 17 is amended as follows:

Amorphous SiC Gate Insulator Embodiment

In one embodiment, the present invention provides a DEAPROM having a storage element including a gate insulator 225 that includes an amorphous silicon carbide (a-SiC). For example, one embodiment of a memory storage element having an a-SiC gate insulator 225 is described in Forbes et al. U.S. Patent application serial number 08/903,453 entitled CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS, filed on the same day as the present patent application, and which disclosure is herein incorporated by reference. The a-SiC inclusive gate insulator 225 provides a higher electron affinity χ_{225} than the approximately 0.9 eV electron affinity of SiO_2. For example, but not by way of limitation, the a-SiC inclusive gate insulator 225 can provide an electron affinity $\chi_{225} \approx 3.24$ eV.

The paragraph beginning at page 23, line 8 is amended as follows:

SiC Gate Material Embodiment

In one embodiment, the present invention provides a DEAPROM having a memory cell 110 that includes a FET 200 having an at least partially crystalline (e.g., monocrystalline, polycrystalline, microcrystalline, nanocrystalline, or combination thereof) SiC floating gate 215. For example, one embodiment of a memory cell 110 that includes a memory storage element having a polycrystalline or microcrystalline SiC floating gate 215 is described in Forbes et al. U.S. Patent application serial number 08/903,486 entitled SILICON CARBIDE GATE TRANSISTOR AND FABRICATION PROCESS, filed on the same day as the present patent application, and which disclosure is herein incorporated by reference. The SiC floating gate 215 provides a lower electron affinity $\chi_{215} \approx 3.7$ to 3.8 eV and smaller resulting barrier energy Φ_{GI} than a polysilicon gate material having an electron affinity $\chi_{215} \approx 4.2$ eV. For example, using a SiO_2 gate insulator 225, a barrier energy $\Phi_{GI} \approx 2.6$ to 2.7 eV is obtained using an SiC floating gate 215, as compared to a barrier energy $\Phi_{GI} \approx 3.3$ eV for a conventional polysilicon floating gate material at an interface with an SiO_2 gate insulator 225.

The paragraph beginning at page 23, line 24 is amended as follows:

According to one aspect of the invention, floating gate 215 is formed from a silicon carbide compound $Si_{1-x}C_x$, in which the material composition x is varied. One embodiment of a memory storage element having a variable SiC composition floating gate 215 is described in Forbes et al. U.S. Patent application serial number 08/903,452 entitled TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE, filed on the same day as the present patent application, and which disclosure is herein incorporated by reference. For example, but not by way of limitation, an SiC composition of about $0.75 < x < 1.0$ yields an electron affinity of approximately between $1.7\ eV < \chi_{215} < -0.4\ eV$. For an SiO_2 gate insulator 225, a barrier $0.8\ eV < \Phi_{GI} < -1.3\ eV$ is obtained. In one such embodiment, floating gate FET 200 provides a data charge retention time on the order of seconds.

The paragraph beginning at page 25, line 20 is amended as follows:

SiOC Gate Material Embodiment

In one embodiment, the present invention provides a DEAPROM having a memory cell 110 that includes a FET 200 having an at least partially crystalline (e.g., monocrystalline, polycrystalline, microcrystalline, or nanocrystalline) silicon oxycarbide (SiOC) floating gate 215. For example, one embodiment of a memory cell 110 that includes a storage element having a polycrystalline or microcrystalline SiOC floating gate 215 is described in Forbes et al. U.S. Patent application serial number 08/902,132 entitled TRANSISTOR WITH SILICON OXYCARBIDE GATE AND METHODS OF FABRICATION AND USE, filed on the same day as the present patent application, and which disclosure is herein incorporated by reference.

The paragraph beginning at page 27, line 1 is amended as follows:

GaN and GaAlN Gate Material Embodiments

In one embodiment, the present invention provides a DEAPROM having a memory cell 110 including a FET 200 having an at least partially crystalline (e.g., monocrystalline, polycrystalline, microcrystalline, nanocrystalline, or combination thereof) gallium nitride (GaN) or gallium aluminum nitride (GaAlN) floating gate 215. For example, one embodiment of a memory storage element having a GaN or GaAlN floating gate 215 is described in Forbes et al. U.S. Patent application serial number 08/902,098 entitled DEAPROM AND TRANSISTOR WITH GALLIUM NITRIDE OR GALLIUM ALUMINUM NITRIDE GATE, filed on the same day as the present patent application, and which disclosure is herein incorporated by reference.